

**MICROCAP WAFER-LEVEL PACKAGE WITH VIAS**

**Inventors:** Richard C. Ruby, Menlo Park; Tracy E. Bell, Campbell; Frank S. Goshay, Cupertino; Yogesh M. Desai, San Jose, all of CA (US)

**Assignee:** Agilent Technologies, Inc., Palo Alto, CA (US)

**Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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**U.S. Cl.:** 438/106; 257/678

**Field of Search:** 438/106, 112, 438/123, 124, 436-459, 612-615; 257/678, 704, 710, 774

**References Cited****U.S. PATENT DOCUMENTS**

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by examiner

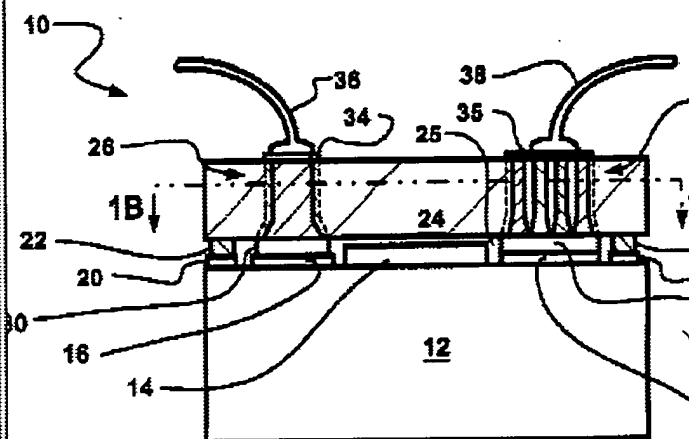
**Primary Examiner—David Naima**  
**Assistant Examiner—Quoc Hoang**

(37)

**ABSTRACT**

A microcap wafer-level package is provided. A micro device is connected to bonding pads on a base wafer. A peripheral pad on the base wafer encompasses pads and the micro device. A cap wafer is provided with a predetermined depth in the cap wafer. A conductive material is made integral with the walls of the cap wafer. The cap wafer has contacts and a gasket formed thereon where the contacts being aligned with the bonding pads on the base wafer. The cap wafer is then placed over the base wafer and the gasket is formed to the pads and form a sealed volume within the peripheral gasket. The micro device is then placed in the sealed volume below the predetermined depth until the dopant is exposed to become conductive and the cap wafer to enclose the hermetically sealed

20 Claims, 8 Drawing Sheets



**DOCUMENT-IDENTIFIER:** US 6228675 B1

**TITLE:** Microcap wafer-level package with vias

**CLPV:**

providing a first wafer, a second wafer, and a micro device ;

**CLPV:**

bonding said first and said second wafers together using said seal to form a hermetically sealed volume therebetween, said second wafer positionable with said conductor in conductive contact with said bonding pad, and said micro device disposed in said hermetically sealed volume and connected to said bonding pad; and

	Document ID	Kind Codes	Source
1	US 20010021570 A		US-PGPUB
2	US 6265246 B1		USPAT
3	US 6255721 B1		USPAT
4	US 6232150 B1		USPAT
5	US 6228675 B1		USPAT
6	US 6094305 A		USPAT
7	US 5966591 A		USPAT
8	US 5831262 A		USPAT
9	US 5481363 A		USPAT

257/678

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**METHOD AND TOOL FOR HANDLING  
MICRO-MECHANICAL STRUCTURES**

Inventor: David D Roberts, Santa Cruz, CA (US)

Assignee: Read-Rite Corporation, Fremont, CA  
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**Related U.S. Application Data**Division of application No. 08/908,648, filed on Aug. 7,  
1997, now Pat. No. 5,966,591.

Int. Cl. H01L 39/72

U.S. Cl. 257/670; 257/347; 257/618;  
257/559; 257/735; 257/773Field of Search 257/618, 347,  
257/670, 669, 735, 773**References Cited****U.S. PATENT DOCUMENTS**

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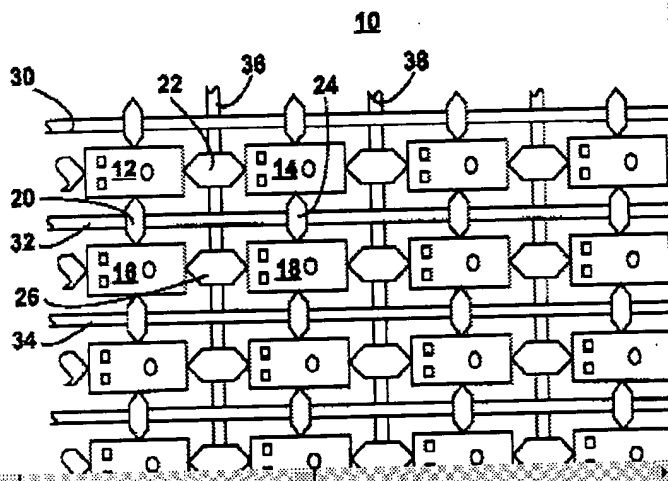
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Primary Examiner—Edward Wojciechowski  
(74) Attorney, Agent, or Firm—Samuel A. I  
(57)**ABSTRACT**

A method of forming and handling an array of such as thin film devices that enables simultaneous handling and processing of these thin film devices of micro-devices and links are assembled on a wafer, with the links interconnecting the devices for maintaining a unitary array structure. A magnetic strips is then formed to impart added strength to the array. The magnetic strips are links and form a planar support grid whereby micro-devices is then released from the wafer, therefrom by means of a magnetic pick-up tool, the array is transferred onto a carrier which securely retains the array. Conductive bonds to a row of micro-devices which are from the array into individual micro-devices.

15 Claims, 7 Drawing Sheets



DOCUMENT-IDENTIFIER: US 6255721 B1  
TITLE: Method and tool for handling  
micro-mechanical structures

CLPR:

4. The array according to claim 1, further including an etchable layer formed on the wafer, intermediate the plurality of micro-devices and the wafer.

CLPR:

5. The array according to claim 4, wherein the plurality of micro-devices are released from the wafer by dissolving the etchable layer.

CLPV:

a plurality of micro-devices formed on a wafer ;

CLPV:

the plurality of micro-devices and the plurality of links being releasable from the wafer .

CLPV:

forming a plurality of micro-devices on a wafer ;

CLPV:

releasing the plurality of micro-devices and the plurality of links from the wafer ;

257/670